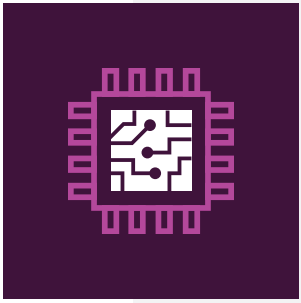

INTEGRATED SUMMARY:

SEMICONDUCTORS

Regaining US competitiveness in semiconductors requires a multi-pronged approach. First, targeted investments in worker training will be necessary to overcome challenging labor and skill gaps in certain regions identified for new leading-edge domestic semiconductor facilities. Second, the US is behind competitor nations in enabling researcher access to commercial production technologies. Firms should be required to increase such access if receiving subsidies for US-based facilities. Last, given the stakes for the economy and security, advances by competitor nations, and funding being insufficient for a broad enough portfolio given uncertainties, the US should increase funding for next-generation (beyond-CMOS) semiconductor devices beyond that in the CHIPS and Science Act.

Type of critical technology assessment Evolving technology with high economic/security impacts; vulnerable supply chain for existing technology

Lead performers Yong-Yeol (YY) Ahn, Christophe Combemale, Hassan Khan, M. Granger Morgan, Neil C. Thompson

Program management Identify the most important problem and problem subcomponents, identify and leverage performers with different methods and disciplines on different components of the problem; midway workshop to elicit stakeholder input and feedback from academia, industry, and government

Methods Expert elicitation, local labor skill gap modeling, productivity measurement, LLMs, engineering-economic models

Data Expert survey results, publications, O*NET data, productivity data from the US Bureau of Labor Statistics, USPTO patent data, the International Technology Roadmap for Semiconductors, and data on CPU and GPU characteristics

Criticality dimensions measured Economic well-being (S&T competitiveness, productivity, jobs)

Challenges for future critical technology assessment Few analysts who can (i) conduct labor constraint analysis, or (ii) pair advanced analytics with deep (non stakeholder) technical and industrial knowledge

Additional contributors: Michael Affare, Tamay Besiroglu, Soojung (Crystal) Chun, Nicholas Emery, Elizaveta Gonchar, Ian Helfrich, Eunji (Emily) Kim, Harrison Leon, Jayson Lynch, Katy Yu

SEMICONDUCTORS

Different disciplines, methods solve *different* aspects of policy problem

SEMICONDUCTORS

Mature and Leading-Edge Semiconductor Devices

FINDING: International academic researchers are increasingly able to access advanced commercial production technologies more than US researchers. This access is necessary for device commercialization.

RECOMMENDATION: The United States should require that companies provide a certain amount of researcher access to commercial facilities in order to receive the currently offered subsidies for investing in US-located leading-edge semiconductor facilities.

FINDING: The gap between workforce supply with relevant skills and those needed for semiconductor fabrication facilities is large in many regions, including in some metropolitan areas that have been earmarked for large scale capability development, causing risks to the investments.

RECOMMENDATIONS: Employers and policymakers should assess the supply of relevant skills as part of the location selection process for large-scale capacity investments. Depending on the specific mismatch between skill demand and supply in a region, targeted skill-specific training programs and incentives to attract new workers to the region should be supported through public-private partnerships.

Next-Generation (Beyond-CMOS) Semiconductor Devices

FINDING: Historically, the gains from improved semiconductors have been large, yielding between $600 billion and $1 trillion in net present value benefits to the US economy per year. As Moore's law ends, these benefits will fade. Beyond-CMOS technologies offer a way to continue improving semiconductors. Potential gains from successful development of these technologies can easily yield trillions of dollars in economic benefits to the US economy, with estimated costs of $100 million to demonstrate and $1 billion to scale up such devices.

RECOMMENDATION: A large portfolio of early- and late-stage post-CMOS technologies should be funded for development at a scale larger than currently allocated in the CHIPS and Science legislation to ensure that the United States develops post-CMOS technologies quickly and before competitors.

Research Questions

What is the optimal implementation of CHIPS funding in semiconductors to achieve the legislation's stated objectives, given financial, technical, and human capital constraints? What is the potential value of investments in next-generation (beyond Moore's law) semiconductor technologies and what investments are needed to overcome bottlenecks to commercialization and scale-up of these technologies?

Motivation/Framing

Improvements to computing are central to American innovation, generating perhaps a third of national productivity growth and underpinning national security. Historically, the United States led the development and deployment of computing, providing military and economic advantage. But technical challenges mean that computing improvement has slowed, so being years ahead of China in computing no longer amounts to as much of a competitive advantage as it once did.

TABLE 4-2. Connection between semiconductor process nodes technology and policy goals

Technology maturity	Mature nodes	Leading edge	Future of compute
Policy goals	Resilient manufacturing supply chains	Competitive US ecosystems	Catalyze and capture emerging tech
Technology	Silicon CMOS		[TBD, "post-CMOS"]
Policy approach	Domestic facility subsidies; international partnerships	Domestic facility subsidies; advanced packaging	CHIPS R&D infrastructure (NSTC, DOD Lab to Fab)
Pilot year demonstration	Assessment and options for addressing labor shortages for regional semiconductor facility build-out		Emerging technology competitiveness; investment portfolio; commercialization and scale-up

China's enormous investments also mean that it has largely closed the advanced computing gap with the United States and is now outpacing US publications on future computing devices that use post-CMOS[1] technologies. If competitive advantage arises from these technologies, it may be China rather than the United States that benefits. Faced with these realities, it is crucial that computing improvement be reaccelerated and that the United States be a leader in developing these technologies.[2]

The CHIPS and Science Act heralds a new era for American semiconductor policy. Policymakers have allocated $76 billion in support for the industry through a combination of manufacturing subsidies ($39B), R&D funding ($13B), and investment tax incentives ($24B). In its allocation of funding and in recognition of the critical role of semiconductors, Congress enumerated a range of desired outcomes, including improving US competitiveness in existing and emerging technologies, strengthening supply resilience for critical industries, and creating jobs. However, Congress was relatively light-handed regarding questions of program design and implementation.

Our pilot year demonstration focuses on how best to implement CHIPS funding in semiconductors to maximize the legislation's stated objectives for security, resilience, jobs, and the economy, given financial, technical, and labor constraints. A variety of semiconductors serve different markets. Semiconductors produced on more mature process nodes often serve safety-critical and robust automotive, aerospace, medical, and military applications; semiconductors on leading-edge nodes tend to applications requiring faster processing and higher performance, like communications and computing. Finally, with the end of Moore's law (the doubling of the number of transistors on a chip about every 2 years), new computing devices are needed to continue progress in a number of applications critical to national and economic security, including AI. As shown in **table 4-2**, in seeking to inform implementation of CHIPS and science legislation, our analyses address the different issues in different types of semiconductors.

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1 CMOS = complementary metal-oxide semiconductor

2 See, for example, Armbrust et al. (2023).

Methods and Sources of Data

The pilot year demonstrations in semiconductors bring together insights from different disciplines and data sources.

SECURING ACCESS TO CURRENT MATURE AND LEADING-EDGE ADVANCED SEMICONDUCTOR PRODUCTS: HUMAN CAPITAL CONSTRAINTS FACING DOMESTIC SEMICONDUCTOR FACILITIES

We develop and deploy a novel capability to assess human capital constraints facing planned domestic semiconductor facilities. We leverage the US Current Population Survey, American Community Survey, and Occupational Employment and Wage Survey to characterize the skill, wage, and occupational distributions for all US metropolitan statistical areas as well as occupation-specific labor mobility. We then assess the gap between the existing skills in each area and the skills required for semiconductor facilities.

ENSURING ACCESS AND LEADERSHIP IN THE FUTURE OF COMPUTE: COMPETITIVENESS IN KNOWLEDGE, COMMERCIALIZATION, AND SCALE-UP

We analyze the US economic benefits of improved semiconductor performance by estimating the share of innovation and hence productivity gains attributable to semiconductors. We then connect these historical gains to improvements in chip-level characteristics, to extrapolate the economic gains from post-CMOS technologies. These estimates can be used to generate optimal portfolios for investment.

We draw on technically detailed interviews with subject matter experts to understand technical bottlenecks and emerging technology capabilities beyond CMOS. The interview questions allowed open-ended responses. An example of our interview protocol and a longer discussion of the method are available under the semiconductors tab on the NNCTA website (nncta.org).

To evaluate country-specific knowledge, commercialization, and scale-up capabilities we used data analytics on a corpus of scientific publications. Our dataset on R&D access to commercial facilities covers 3,500 papers published in the *Journal of Solid State Circuits* from 2012 through 2022. For each paper we manually coded institution type, technology used, and type of collaboration to enable more granular analysis. The data yield a quantitative view of scientific knowledge in specific subfields as well as country-specific access to commercial production facilities for scale-up.

Integrative Findings

SECURING ACCESS TO CURRENT MATURE AND LEADING-EDGE ADVANCED SEMICONDUCTOR PRODUCTS: HUMAN CAPITAL CONSTRAINTS FACING DOMESTIC SEMICONDUCTOR FACILITIES

Depending on the region, the successful realization of public and private investments in building out new domestic semiconductor facilities may face significant human capital constraints. Conversely, where proposed sites have strong labor markets for the relevant manufacturing skills, the new facilities may erode the skill supply for incumbent industries, potentially creating labor constraints and corresponding supply chain risks. As shown in **figure 4-10**, these human capital constraints might be resolved through broader-based talent recruitment and training, including targeting nontraditional industry sources from occupations with less similar skill sets (Columbus, Ohio). However, even relaxing the skill similarity may not solve the skill deficit in some regions (e.g., Sherman-Denison, Texas).

ENSURING ACCESS AND LEADERSHIP IN THE FUTURE OF COMPUTE: COMPETITIVENESS IN KNOWLEDGE, COMMERCIALIZATION, AND SCALE-UP

There is great economic value in investing in demonstrating, commercializing, and scaling up post-CMOS technologies as soon as possible because improved semiconductors will yield innovations that permanently improve productivity.

Each year of delay in developing post-CMOS technologies forgoes near-term benefits, costing the US economy hundreds of billions of dollars. Our economic analysis reveals that the costs of developing post-CMOS technologies (early results from expert interviews suggest about $100 million in dedicated funding for a novel post-CMOS technology to reach the demonstration stage [roughly equivalent to Technology Readiness Level 5-6]) are small compared to the prospective benefits, which could easily be many trillions of dollars in net present value terms.

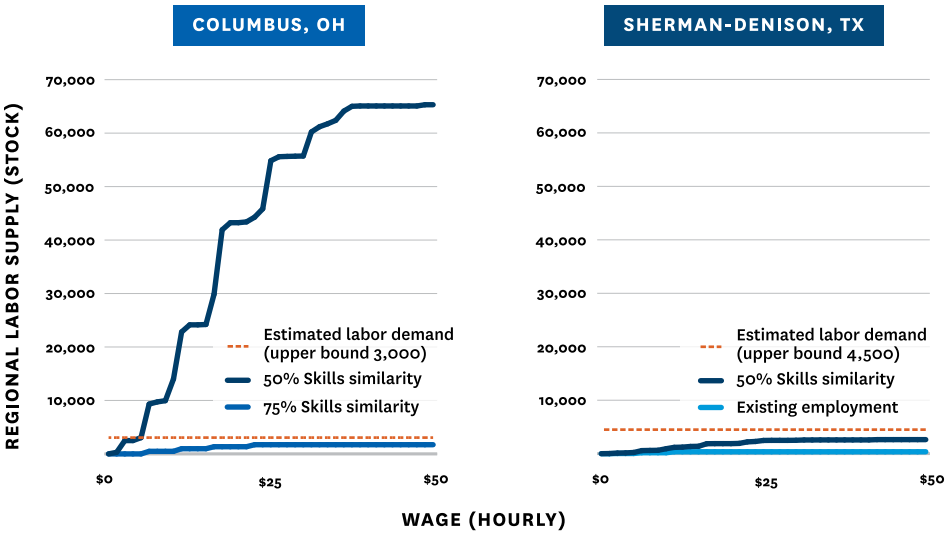

FIGURE 4-10. Availability of employees with skills similar to those needed for a proposed semiconductor manufacturing facility in Columbus, Ohio, and Sherman-Denison, Texas.

While today it is unknown which beyond-CMOS technologies will be successful, the potential economic benefit suggests that investing in a broad portfolio of early-stage technologies, even at costs of tens of millions of dollars each, holds high potential returns. Many later-stage technologies should also be funded, despite being more expensive, because the benefits of even a single success justify a portfolio of investments.

The share of US-based publications leveraging advanced production technologies declined significantly from 2017 to 2022 (**figure 4-11**). Our analysis of over 3,000 papers in the *Journal of Solid State Circuits* suggests that foreign researchers, in both industry and academia, are increasingly able to access the leading-edge commercial production technology needed to move from a demonstration to a commercially viable product.

Options and Tradeoffs for the US Government

US policymakers should assess workforce capabilities in regions targeted for semiconductor facility investment and coordinate with firms and local, state, and federal governments to assess skill and labor gaps and associated region-specific occupation-transition training opportunities. Region-specific public-private partnerships will likely be the best method to address those needs.

Two policy tradeoffs of note emerge from the findings of our pilot year demonstration. First, in the case of R&D infrastructure spending, policymakers will need to find a balance between funding prototyping facilities and investing in researcher access to the type of commercial production facilities necessary for scale-up. In the United States there is considerable focus on building prototyping capabilities with investments at university or nonprofit entities. But it is unlikely that these facilities will be able to support the full commercial production flows necessary to go from demonstration of a beyond-CMOS device to development for commercialization.

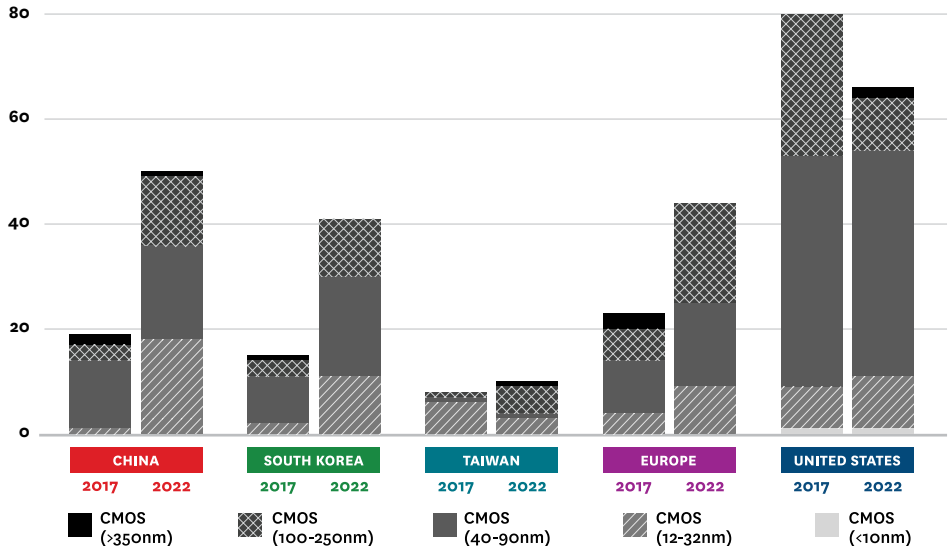

FIGURE 4-11. International economic competitors are increasingly better equipping academic researchers for commercial development.

That said, prototyping facilities have benefits: they are a lower-cost investment than later-stage technology development and so can be implemented at more locations and in different device material systems across the nation with a fixed amount of funds (instead of an investment in a more costly facility to continue development of a technology for commercialization). Limited funds thus allow a greater portfolio of devices to be demonstrated. In addition, prototyping facilities at multiple universities, each for different device materials systems—more numerous than a single later-stage emerging device scale-up facility—offer training opportunities for more students and skilled labor across more geographic regions. For commercial scale-up, the CHIPS office, in implementing the proposed National Semiconductor Technology Center (NSTC), might identify technology nodes and flows with a breadth of applications and look to secure design kits, test structure, and process design kits to enable those at a single closer-to-commercialization prototyping facility. An alternative, lower-cost option emerged from our findings: Instead of a single NSTC, the CHIPS office might focus prototyping funds on upgrading existing university facilities and incentivizing firms—as part of receiving subsidies for US-based semiconductor facilities—to dramatically improve their shuttle run and MPW offerings for US researchers. The specific program for improving shuttle run and MPW offerings could then be executed in coordination with the National Semiconductor Technology Center (NSTC). This option is particularly attractive since beyond-CMOS technologies will likely find their earliest commercialization opportunities in existing CMOS-centric designs (such as application-specific accelerators).

Second, our demonstrations highlight a tension between the spending allocated in the CHIPS and Science Act for semiconductors and the costs of pursuing emerging technologies with potentially massive societal benefits. Experts estimated the costs to bring an emerging beyond-CMOS technology to readiness stage 5 to be on the order of $1 billion. Even with the act's historic spending amounts, it would not be feasible to bring more than one or two technologies to that stage absent private funding or strong complementarities between the technologies. Because of the scale of the benefits from post-CMOS technologies, and the strategic importance of US leadership in cutting-edge computing, we recommend that funding for the development of novel computing technologies be made available.

Vision for Future Analytic Work

The NNCTA's semiconductor research and demonstrations in the pilot year focused on implementation of the stated goals and objectives of the semiconductors portion of the CHIPS and Science Act, given funds allocated and technical and human capital constraints. Continued NNCTA capability could help policymakers answer the question of "what policy responses can help America close the gap in leading-edge semiconductor production capabilities?"

Looking forward, our goal is to build a critical technology analytics capability that is strategic and forward looking. We hope to anticipate emerging challenges in semiconductor policy, enabling policymakers to be proactive. To that end we are working with the Network's situational awareness team on broader and deeper assessments of international research capabilities. This work will include evaluation of different institutional models and possible lessons for the design and operation of the NSTC.

It would also be important for the NSTC to promote a broader, more comprehensive survey of experts than is currently provided by the IEEE International Roadmap for Devices and Systems (IRDS), to generate more detailed and comparable assessments of the promise of each technology. For context, the IRDS covers 14 categories of post-CMOS technologies; of these, only 8 have quantitative estimates for their technical potentials. A full list, with better uncertainty quantification, is needed.

Enhanced understanding of the labor dimensions of critical technology challenges in semiconductors requires further estimates of the flow and elasticity of labor supply, to capture the timeline over which skills may become available. Our assessment currently relies on measures of similarity in occupational skill requirements; these measures need to be validated against empirically observed rates of transition. This approach will require further analysis of the costs of (i) training or other interventions to facilitate transitions across skill gaps between occupations and (ii) turning potential labor supply into a realized occupational transition.

Another potential area for future work is deeper supply chain analytics. However, data availability challenges must be overcome. The independent NNCTA may offer a solution to concerns about data sharing between industry competitors. But decades of outsourcing and offshoring have resulted in limited visibility into extensive and multilayered international supply chains, especially in complex products such as automobiles and defense systems. Assuming such data challenges can be overcome, analytics can help provide insight into what types of chips are most critical for reducing risky overreliance on foreign manufacturers. Today these questions are difficult for policymakers to answer at an industry level and impossible to answer at the economy level.

Potential Broader Lessons for Critical Technology Assessment

Economic analyses can provide order-of-magnitude estimates that are crucial for understanding the scale of investments and breadth of technology portfolio needed to maximize the benefits to the US economy. While manufacturing capabilities have been the focus of global comparisons in semiconductors there is evidence that international researchers are reducing the capability gap with US researchers, in part through better access to commercial production technologies, especially in China. This suggests that US investments in R&D infrastructure need to encompass both dedicated noncommercial facilities and access to industry facilities. This framing requires thinking about R&D and manufacturing capabilities in conjunction with each other and not as separate programs.

Substantial variability in US regional skill supply is a potentially binding constraint on the viable development of critical technology capabilities. Strategies that include diffusion of technology for greater economic inclusion will require place-based assessments of skill readiness and the development of corresponding approaches to address disparities. There may be tradeoffs between regions that are most ready to participate in technology capability building and those most in need of resources to enhance economic prosperity and equity.