National Network
For Critical
Technology Assessment

Hassan Khan

Federal Investments in Semiconductor Fabs Should Include Researcher Access

BLUF: As the Biden Administration provides almost $39B in incentives to build semiconductor fabs in the US, they should ensure these fabs and their community benefit agreements guarantee "research access" to allow testing of next-generation technologies and training of future researchers and practitioners. If the US is to maintain its standing as the world leader in semiconductor R&D, we need to ensure researchers have access to commercial production lines.

Background

- The growing complexity and capital intensity of modern semiconductor production means that commercial production infrastructure is also critical research infrastructure.
- An analysis of >10 years of publications in the IEEE Journal of Solid State Circuits shows that an increasing portion of published papers leverage commercial processes for their work and that the US is falling behind on research access, with a larger portion of papers published by authors from China, South Korea, and Taiwan being done on advanced CMOS nodes than those in the US even though the US still publishes the most papers.
- Researchers and start-ups often need to use "multi-project wafers" (MPWs) as the most cost-effective way to test their designs, on top of commercial production lines at foundries.
- However, MPW support in the U.S. is fragmented, and firms push those runs due to commercial considerations. Collectively, this lack of access is setting us up to lose the race for global leadership.
- If the US is to maintain its standing as the world leader in semiconductor R&D, we need to ensure researchers have access to commercial production lines on a regular basis and with appropriate associated support to lower barriers of entry.

Opportunity

- CHIPS represents a major reset opportunity. As we look to expand our production footprint in the US, we should also ensure it benefits our academic, research and startup communities. One approach to doing so is requiring firms who receive subsidies from the CHIPS program to ensure these users have access to affordable MPW runs.
- The Administration should do two things.
- First, any federal subsidy of a fab facility and community benefit agreement should include a research access provision. This should include the following components:
    - Free/low cost quarterly MPW runs. It is critical these MPW runs are available on a range of process nodes including leading-edge finFET and mature nodes.
    - Collateral IP support for the MPW runs including std cells, IO cells, memory compiler, memory interface, chip to chip interface, basic analog blocks, PLL, etc.
    - Training materials for the MPW runs as well as collateral IP for interface and test.
    - Access to advanced packaging (2.5D interposer, EMIB, HBM, etc.)
    - No lock out periods on NDAs

- Second, the Administration should take steps to ensure broad access for researchers to this opportunity. This should include:
    - Firms developing robust training material and collateral IP to ensure a range of academic institutions and researchers have access to MPWs.
    - Firms required to include proposals for MPW support, including detailing their training material, collateral IP, and community engagement plans as part of the subsidy RFP
    - Active involvement of the NSTC as a central point of support for coordinating the academic and research community's access to MPWs across US fabs. This can reduce the operational burden on firms while also encouraging the development of standardized processes to reduce the burden on users. As a first step, the NSTC should fund a survey of academics, start-ups, and researchers of their MPW support and technology needs.

Ultimately, this tie-in between CHIPS manufacturing funding and R&D infrastructure will help ensure our investments are mutually reinforcing. Ensuring the US community has access to commercial fabs to build their ideas will accelerate innovation and human capital development. Creating a coordinated infrastructure within the NSTC will lower the barrier to entry and allow more users across the country to build chips from their own designs. These will in-turn benefit the firms who provide access by creating new pipelines for ideas and talent.

National Network
for Critical
Technology Assessment

APPENDIX

All data below is only for academic authors